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# A STUDY OF WAVE PIPELINED CIRCUIT FOR AN LDPC DECODER

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## ABSTRACT

Wave-pipelined circuits offer a promising approach to enhancing the performance of Low-Density Parity-Check (LDPC) decoders, which are crucial in error correction for digital communication systems. Unlike conventional pipelining, wave pipelining doesn't require intermediate registers between stages. Instead, it relies on careful timing to ensure that data waves propagate through the circuit without colliding. This method allows for higher throughput, as multiple data waves can be processed simultaneously, increasing the overall speed of the LDPC decoding process. In an LDPC decoder, which typically involves complex iterative algorithms and substantial data processing, the speed and efficiency of the circuit are paramount. Wave pipelining can significantly reduce the latency of these decoding operations by minimizing the clock cycle time and maximizing the utilization of the circuit's resources. This is particularly beneficial in high-speed communication systems, such as 5G networks, where fast and reliable error correction is essential. Moreover, by reducing the need for additional hardware (like registers), wave-pipelined circuits can also contribute to lower power consumption and smaller chip area, making them an attractive solution for implementing LDPC decoders in resource-constrained environments.